32.2 A Low Phase Noise 10GHz Optoelectronic RF Oscillator Implemented Using CMOS Photonics

Cary Gunn[1], Drew Guckenberger[1], Thierry Pinguet[1], Deana Gunn[2], Danny Eliyahu[2], Barmak Mansoorian[3], Daniel A. Van Blerkom[3], Olli Salminen[3]

[1]Luxtera, Carlsbad, CA, [2]OEwaves, Pasadena, CA,
[3]Forza Silicon, Pasadena, CA

The emerging wireless communications standards at higher frequencies, especially toward 60 and 80GHz, are challenged by the availability of cost-effective high performance oscillators. Since the bandwidth of a wireless communications system is heavily dependent on the phase noise of the local oscillator, spectral efficiency at these frequencies is limited to a fraction of that achieved in cellular, WiFi, and WiMax applications using available local oscillators (LO). LO performance also limits the precision of radar systems, such as mm-wave phased array radars.

It has been known for some time that an optoelectronic oscillator (OEO) can achieve better phase noise performance than traditional frequency synthesis approaches, such as phase-locked dielectric resonators, YIG, and quartz crystal oscillators [1,2]. The fundamental improvement in phase noise achievable in an OEO is attributable to direct frequency generation from an optical source rather than through electronic multiplication. OEO systems, however, are historically assembled from discrete devices and therefore require large volume and power consumption, and result in high cost. Additionally, there are vibration problems encountered with the assembly of a large number of discrete parts, an issue for both commercial and military environments. Described here is the integrated implementation of this optoelectronic circuit in Luxtera's 130nm SOI CMOS photonics technology [3], resulting in a low power, small footprint implementation of the OEO with low phase noise.

Two coupled loops create the OEO (Fig. 32.2.1), one providing RF gain, and the other providing optical gain. The optical loop is essentially a mode-locked laser with an extremely long optical delay placed in the optical cavity. The RF loop provides the RF output signal and reinforces/determines the operation frequency of the OEO. The long optical delay creates high spectral purity and low phase noise, and is achieved with either a high Q optical resonator or a long length of fiber with an equivalent delay. The optical loop consists of a silicon Mach-Zehnder Interferometer (MZI) modulator in series with a semiconductor optical amplifier (SOA) and the optical delay element (ODE), in this case a fiber coil. The output of the fiber is connected back to the input of the modulator, completing a loop with positive gain. The MZI was optimized for this application by ensuring that adequate bandwidth and extinction ratio were achieved with low optical insertion loss (< 4dB).

A portion of the optical energy is tapped from the loop and directed to a photodetector (PD), which feeds the RF feedback path. Figure 32.2.2 shows the locking of the optical modes, spaced by 10GHz, which are converted to a 10GHz RF signal at the PD. The signal from the PD is amplified using a CMOS low-noise amplifier (LNA), filtered at the frequency of operation with a bandpass filter (BPF), and returned to the optical modulator driver. A voltage-controlled phase shifter (VCPS) ensures adequate phase alignment between the two closed loop systems. The circuit was designed to oscillate at 10.24GHz, with an output RF power of 0dBm.

A differential LNA and BPF create the first two stages of the RF signal chain, and are shown in Fig. 32.2.3. The LNA uses on-chip spiral 1.0nH inductors at its input to achieve a narrow-band match to 50Ω at 10.2GHz. The LNA is cascoded and has on-chip inductive loads of 1.35nH. The input and cascode NMOS devices are non-body tied for the highest f_T, while the bias devices are all body-tied. The LNA has a peak gain of 23.2dB at 10.2GHz and the -3dB bandwidth is 2.6GHz. The power dissipation is 9.6mW, and the layout area is 0.15mm^2. The stand alone LNA has a measured phase noise of -140dBc/Hz at a 10kHz offset from the carrier.

The BPF consists of a cascoded, degenerated differential pair with inductive loads in parallel with PMOS varactors. The center frequency of the BPF is adjusted by adjusting the body-tied bias of the PMOS varactors. The quality factor of the BPF is adjusted by adjusting the bias current of the negative Gm stages shown in Fig. 32.2.3. Two of the negative Gm stages are unbalanced to maintain a constant Gm with large signal swings [4]. The measured BPF response is shown in Fig. 32.2.4. The filter bandwidth is tunable from 400MHz to 1.15GHz and the center frequency is tunable by 200MHz.

The I/Q-based VCPS concept is shown in Fig. 32.2.5. The incoming signal is split into two branches with a two-stage polyphase filter, which generates two outputs with a fixed 90° phase shift between them. The phase rotation from 0° to 90° is achieved by adjusting the amplitudes of the two branches separately using VGA stages. Any phase shift between these two extremes is possible and the resolution is defined by the amplitude control step of the VGAs. The VGA design is a CMOS implementation of a well-known current division based VGA concept presented in [5]. Since the outputs of the VGAs are currents, they can be summed together using just two shared inductors as loads. The phase control range is extended to cover 360° by swapping the polarities of the VGA stage outputs (0 or 180°). In this design the phase shifter quadrant is selected with two control bits and the precise phase shift within the quadrant can be adjusted with two analog continuous VGA control signals. This phase shifter concept does not rely on LC resonance for phase adjustment and is therefore fairly broadband and insensitive to absolute component tolerances.

The fabricated chip in Fig. 32.2.7 shows two partial OEO circuits designed on a single die. The two circuits are identical with the exception of two different VCPS designs, only one of which was discussed above. The chip was packaged and the optical ports were fiber pigtailed. Completing the circuit with an external ODE and an SOA, optical locking and RF oscillation at 10.2GHz was achieved. The system phase noise was -112dBc/Hz at a 10kHz offset (Fig. 32.2.6). The performance is limited by the RF electronics (using external RF components and an integrated Si optical loop, a phase noise of -139dBc/Hz at 10kHz has been achieved). The open loop RF phase noise was -125dBc/Hz at 10kHz offset. The oscillator phase noise is anticipated to improve significantly with improved RF component design.

Besides the dramatic change in size and weight of the OEO portion that was integrated, there was a significant decrease in the RF power consumption of the integrated versus the discrete version of the OEO. While in the discrete off-the-shelf component version, the RF amplifiers may use as much as 10-20W, the entire integrated RF chain uses less than 200mW. The integrated components operate from a 1.2V power supply and do not need the matching input and output drivers that discrete components require. The modulator driver typically uses 575mW.

This work demonstrates a dramatic reduction in the size, weight, and power of the OEO, using a platform that monolithically integrates optics and RF electronics and is a successful proof-of-concept of opto-electronic oscillator integration in silicon.

References:

[1] X. S. Yao, and L. Maleki, "Optoelectronic Oscillator for Photonic Systems," *IEEE J. of Quant. Elec,* vol. 32, pp. 1141-1149, July, 1996.
[2] X. S. Yao, L. Davis, and L. Maleki, "Coupled Optoelectronic Oscillators for Generating both RF Signal and Optical Pulses", *IEEE J. of Lightwave Tech.*, vol. 18, pp. 73-78, Jan., 2000.
[3] B. Analui, D. Guckenberger, D. Kucharski and A. Narasimha, "A Fully Integrated 20-Gb/s Optoelectronic Transceiver Implemented in a Standard 0.13μm CMOS SOI Technology," *IEEE J. Solid-State Circuits*, vol. 12, pp. 2945-2955, Dec., 2006.
[4] D. L. C. Leung, and H. C. Luong, "A Fourth-Order CMOS Bandpass Amplifier with High Linearity and High Image Rejection for GSM Receivers," *Proc. ISCAS*, vol. 2, pp. 589-592, May, 1999.
[5] W. M. C. Sansen, and R. G. Meyer, "Distortion in Bipolar Transistor Variable-Gain Amplifiers," *IEEE J. Solid-State Circuits*, vol. 8, pp. 275-282, Aug., 1973.

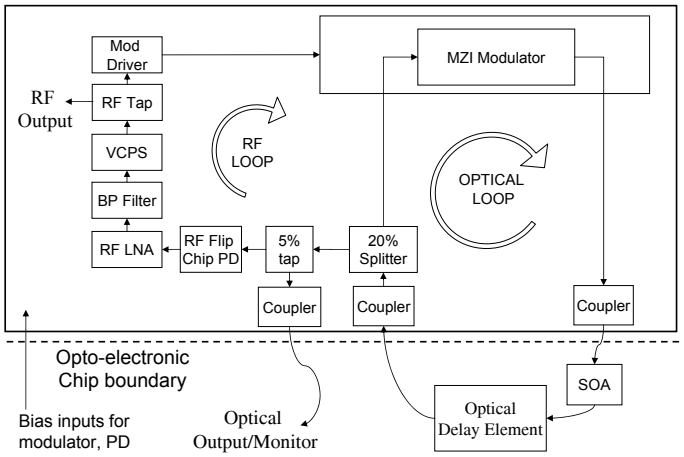

Figure 32.2.1: System architecture.

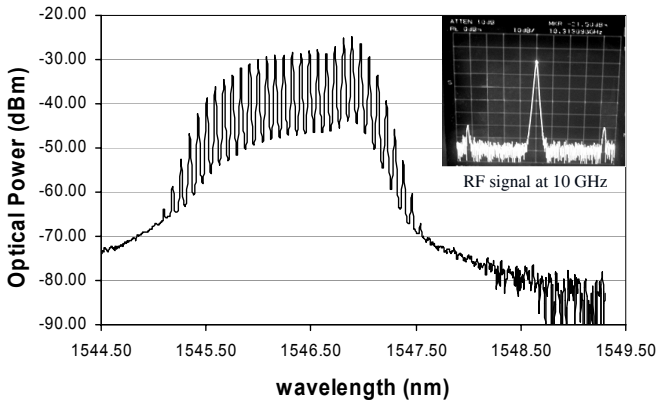

Figure 32.2.2: Optical locking of 10GHz-spaced modes, and corresponding 10GHz RF signal.

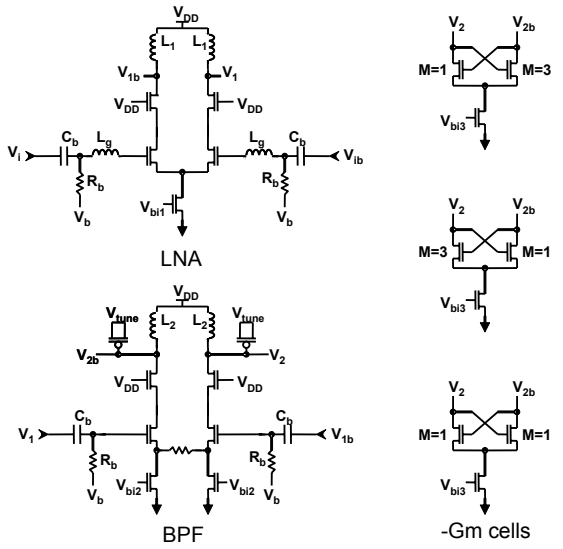

Figure 32.2.3: LNA and BPF circuit schematics.

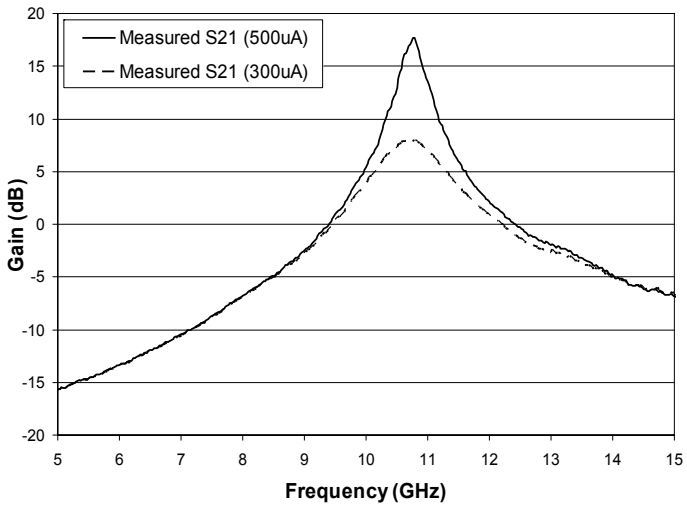

Figure 32.2.4: Stand-alone BPF response with Q tuning.

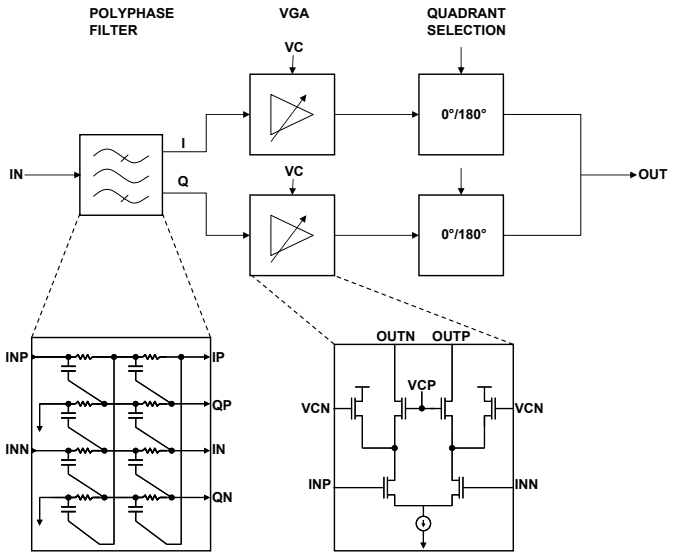

Figure 32.2.5: VCPS circuit schematic.

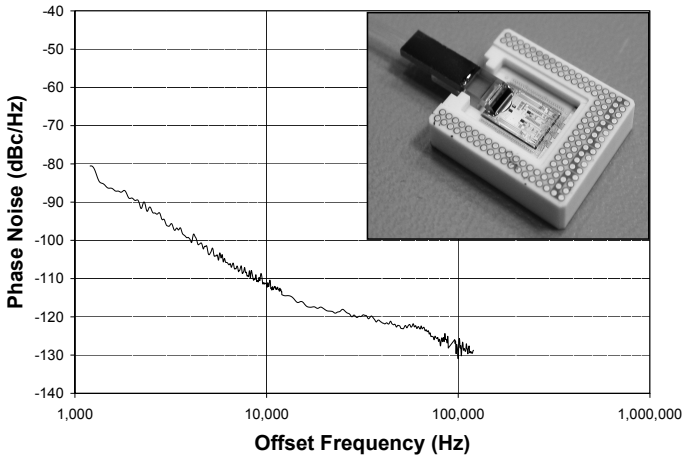

Figure 32.2.6: Closed loop OEO phase noise at 10GHz using the packaged chip coupled to an external SOA and ODE.

Continued on Page 622

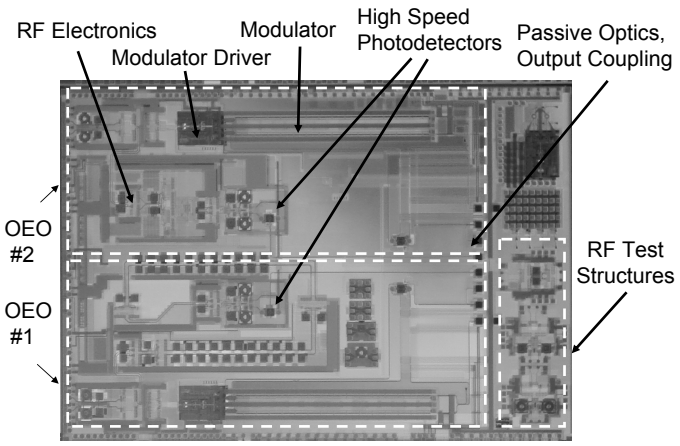

Figure 32.2.7: Die micrograph, containing two side-by-side OEO circuits on a 5x8mm² die.

